

Asynchronous I/O PMC

32-Channel Digital I/O Board w/TimeStamp

The Technobox 32-Channel Digital I/O board provides 32-bits of bi-directional CMOS-level (TTL compatible) I/O available at the JN4 connector on a PCI Mezzanine Card.

The 32-bits are individually programmed for direction - either input or output - by a 32-bit register written by the host processor. A 56-ohm series terminator is provided for each line. When reset, all 32-lines default to inputs, but are biased low by 10K ohm pull-down resistors.

The 32 bits are accessed in parallel using programmed I/O via the PCI slave-only bridge. All 32-bits are simultaneously read in parallel, including those bits programmed as outputs. All 32-bits can be written simultaneously in parallel, selectively set, or selectively reset for those channels programmed as outputs.

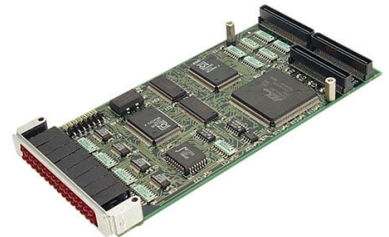
The state of each digital I/O signal is visible via LEDs located at the PMC front-panel, and

provide a convenient means of determining nominal signal levels on all 32-bits. The LEDs are buffered from the digital I/O lines, essentially presenting no load to the lines.

An additional feature of this board is a 30-ns timestamp. Whenever a change in state occurs on any of the 32-bit digital I/O lines, the hardware detects the change in state and writes all 32-bits into a FIFO, along with a 16-bit timestamp counter.

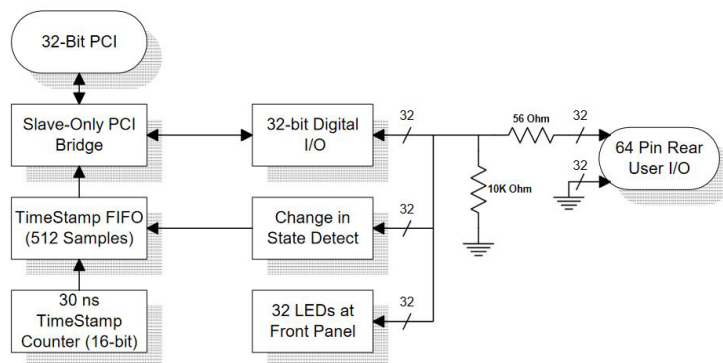
The timestamp FIFO is accessed via programmed I/O from the PCI bus. The 512 timestamp word storage capacity of the FIFO permits correct capture of several closely-spaced digital I/O events. Accordingly, 30-ns resolution is maintained, and the actual load incurred by the host program depends on the amount of activity on the digital I/O lines.

The timestamp FIFO is also written whenever the 16-bit timestamp counter rolls over (i.e., every 2 milliseconds). This

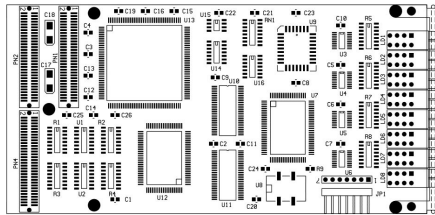


2195

- RoHS-compatible
- Lead-free



Technobox[®], inc.



COMPONENT PLACEMENT VIEW - SIDE #1

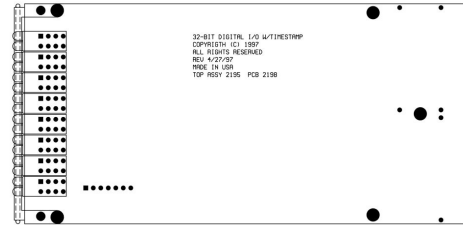
allows timing to be maintained on infrequently changing digital I/O.

The FIFO “watermark” is programmable from the host processor. When the number of samples in the FIFO exceeds the watermark level, an interrupt is asserted on the PCI bus. The interrupt handler can then read the number of valid samples as indicated by the watermark number.

Each of the 32 digital I/O lines

has a corresponding GND which is connected to the 64-pin JN4 connector on the PMC. The host processor must support PMC rear I/O connection per the IEEE 1386 CMC specification in order to allow access to the digital I/O on the VMEbus P2 connector “a” and “c” rows. The pin-out is such that an IDC ribbon connector used for P2 results in alternating signal/ground conductors in the ribbon cable.

For cost-reduced applications, the LED indicators and/



COMPONENT PLACEMENT VIEW - SIDE #2

or timestamp hardware can be removed on special production builds of this board. Contact Technobox for your special requirements.

SPECIFICATIONS

Temperature (Operating): -40 to +85 degrees C

Temperature (Storage): -40 to +100 degrees C

Altitude: Not Specified or Characterized. Typical similar equipment is at 15,000 ft.

Humidity (Operating/Storage): 5% to 90% non-condensing

Vibration: Not Specified or Characterized.

Shock: Not Specified or Characterized.

PCI Environment: 5 Volt

ORDERING INFORMATION

2195: 32-Channel Digital I/O Board w/TimeStamp

