Feature Comparison: P/Ns 2674, 4289, 4792, and 7757

Feature	P/N 2674 "Original" Product	P/N 4289 "Enhanced" Product	P/N 4792 VITA 20 ccPMCC "Enhanced" Product	P/N 7757 XMC - VITA 42 "Advanced" Product	Discussion
FPGA	FLEX 10K70-4	Cyclone EP1C12F324C8	Cyclone EP1C12F324C8	Cyclone 5CGXFC4C6F2717N	Changed from FLEX to Cyclone family. Cyclone 1 for PMC, Cyclone V for XMC.
Logic Elements	3744	12060	12060	50,000 equivalent LEs (18,860 ALMs)	Per ALTERA datasheets. Design uses "migration" to support higher density if needed.
Embedded Array Blocks	9 (2048x1b to 256x8b)	52 (4096x1b to 128x32b)	52 (4096x1b to 128x32b)	2.5Mbits in M10K blocks 678Kbits in MLAB blocks	Progression of higher internal SRAM per Altera FPGA evolution
SRAM on PLX Local Bus	128Kx32b in 4 chips	256Kx32b in 2 chips	256Kx32b in 2 chips	256Kx32b in 2 chips accessed from FPGA	Enhanced product doubles SRAM capacity located on the PLX local bus. Retained for XMC
PCI Interface	33 MHz, 32b 3.3V or 5V signalling	33/66 MHz, 32/64b 3.3V or 5V signalling	33/66 MHz, 32/64b 3.3V or 5V signalling	Two GEN 1 (2.5 Gb/s) PCI Express links connected directly to FPGA	Switch from external PLX parts for PMC to internal IP hard core in Cyclone V for XMC
PCI Chip	PLX 9080	PLX 9656	PLX 9656	Internal PCIe hard core in FPGA	Next generation PLX interface is highly backward compatible with 9080 chip. XCM moves to non-PLX implementation.
Local Bus Clock	Either 24 or PCI bus (33 MHz) per resistor population	24, 33, 50, or 66 MHz per resistor population	24, 33, 50, or 66 MHz per resistor population	N/A; Generally FPGAS implementations will have an internal "Avalon bus" running at appropriate bus speeds, perhaps slaved to PCIe speed	PLX 9656 is capable of up to 66 MHz local bus clock operation. Actual speed achievable depends on FPGA design details. 24MHz (default) retained for backward compatibility.
Local Bus Width	32b	32b	32b	Per internal FPGA implementation	No change to local bus width.
Byte Accessibility and Direct Master	32-bit only, no direct master	Supports LBE lines and "direct master" mode	Supports LBE lines and "direct master" mode	N/A; Internal Avalon bus supports various partial bus transfers and bus widths as needed for application	Enables byte accessibility to PLX local bus devices and allows for bus mastering to the PCI bus through the 9656. N/A for XMC.
Differential Transceivers	SN75976A1DL	SN75976A1DL	SN65HVD10Q (rated for -40 to +125 degrees C	SN65HVD10Q (rated for -40 to +125 degrees C	No change in RS485/422 interface chip. However, Vita 20 ccPMC and XMC uses 1channel device with extended temperature range.
Differential Termination	Parallel 120 ohm	Parallel 120 ohm	Parallel 120 ohm	Parallel 120 ohm	No change from original design
Load FPGA Image over PCI Bus	Yes	Yes	Yes	Yes; via Altera CVP mode (seeAltera dcoumentation for more details)	Enhanced design allows same over-the-PCI bus FPGA initialization as original design. XMC adopts ALTERA's "CVP" strategy.
Load FPGA via On-board PROM	Via EPC1 one-time programmable socketed part programmed via special programmer	Via EP1CS4 in-circuit programmable part; programmed via Altera ByteBlaster II	Via EP1CS4 in-circuit programmable part; programmed via Altera ByteBlaster II	Via 64Mbit N25Q064 quad serial flash memeory. Programmable via Altera USB Blaster, etc.	Easier to use in-circuit re-programmable EP1CS4 part for automatic power-up configuration of FPGA. XMC uses 4-bit wide part to achieve 100ms configuration per PCI-e requirements.
Load FPGA via JTAG Signals on PMC Bus	No	Yes	Yes	No; JTAG access is always done via a USB Blaster (or equivlent) plugged into back of XMC board	Convenient for development/debug cycles. JTAG connector is available on Technobox P/N 3390 and other adapters. Not supported on XMC.
ByteBlaster II / USB Blaster Support	No	Yes	Yes	Yes; via "thru-the-board" header. (see product manual)	On enhanced product, both JTAG and In-Circuit programming headers are provided.
20-pin Logic Analyzer Header	Yes	Yes	Yes	No; however, there are ten "spare" signals on edge of board tht can be used if needed for real logic analyzer	No change here. Also, Cyclone family supports embedded "signal tap" logic analyzer via JTAG.

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PLL clock generators	ICS1522	ICS1522 + 2 internal	Cyclone Internal ONLY. (No ICS1522 external PLL chip is available on the ccPMC board)	Cyclone Internal ONLY. No external PLLs are provided.	Retained ICS1522 PLL chip for backward compatibility, but Cyclone also supports two internal PLLs which are supported in the enhanced design. Conduction Cooled Version does not have ICS1522 available.
Front Panel I/O	Yes	Yes	No	Yes	No change in signals for front panel I/O. Conduction Cooled Version has Rear I/O (PN4) only.
Rear I/O (PN4)	Yes	Yes	Yes	Yes (via PN4, no P16 support)	Front Panel I/O electrically connected to Rear I/O (PN4). No difference between original and enhanced products
Delay Lines	Two 100ns, 5 tap	Two 100ns, 5 tap	Two 100ns, 5 tap	Two 100ns, 5 tap	Two 5-tap, 20ns/tap (100ns total) delay lines retained for enhanced design.
More On-board LEDs	2	4	4	5 (4 "user" + 1 "Lane Active")	A few more FPGA-controlled LEDs for status and debug convenience on "enhanced" products.
Provision for Specialty Oscillator	No	Yes	Yes	Yes	New design allows customer population of 14pin DIP oscillator for precision applications (TXCO, OXCO, VXCO, etc). Oscillator Voltage Control (VC) A:D is included.
EEPROM	No	Yes	Yes	Yes	Serial EEPROM connected to FPGA for user related power-up configuration and the like.
Temperature Sensor	No	Yes	Yes	Yes	Temperature sensor (located in RS485 Transceiver area) for monitoring operating temperature conditions.
Conformal Coating	Optional	Optional	Standard	Optional	Conduction Cooled version has Acrylic Conformal coating as standard deliverable.
IC Temperature Range	0 to 70 degrees C.	0 to 70 degrees C.	-40 to +85 degrees C.	-40 to +85 degrees C.	Conduction Cooled version employs chips that are rated for at a minimum Industrial Temperature Range (-40 to +85); Users may need to de-rate according to system heat flow.
Power Supply Required	5V only	5V only	3.3V only	3.3V. "VPWR" (either +5V or +12V) is needed if "Specialty Oscillator" is in use. VPWR is a standard XMC voltage rail and should always be available.	Although enhanced design uses mixed 5V/3.3V logic, an on-board regulator generates the local 3.3V requirements so that only 5V applied to the board is all that's needed. Conduction Cooled Version requires 3.3V only.
Design Tool	Max Plus II or Quartus 3.1 or later	Quartus 3.1 + only	Quartus 3.1 + only	Quartus tools that support Cyclone V FPGAs.	Use of Cyclone requires movement to Quartus. Altera makes this automatic. As part of migration, users will need to re-assign pins and also incorporate minor changes to FPGA design.
Price	$1195	$995	$1495	$1195	This is single piece list price. Quantity discounts start at 2 pieces and are based on a discount formula. Contact Technobox for more pricing information.

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