FPGA Migration Instructions for PN4289 to PN9136

Technobox Reference Design PN9136

The PN9136 default reference design programmed into the serial Flash was compiled using Quartus Lite 18.1. It is the PN4289 reference design with the following minor changes (no operational impact):

- HOLDA and I/O interrupt signals are synchronous
- PLL's are reset by FPGA reset
- Read only control register bits were added (refer to example SW).

FPGA Migration

Perform the following steps to migrate your design

- Determine which Quartus version to use
- Create a duplicate directory of the existing design
- Run the Technobox FPGA Migration Tool available from www.technobox.com
  Note: The Migration Tool updates the Quartus Project Device and Pin Assignment statements, it does not make any other project or design changes.
  - Select your QSF Project file and the "PN4289 -> PN9136" Tech Refresh Migration option
  - select the "Migrate" button to update the file.
- Open the updated Project and review any warnings / errors reported from opening the project
- Recommended: Review or upgrade any Altera IP
- If applicable, convert from the ICS1522 PLL to an internal Cyclone V PLL
- If applicable, convert from EPCS4 to EPCQ128
- If applicable, upgrade from SOPC Builder.
- If applicable, convert from Classic Timing Analyzer
- Recommended: Review pin settings such as Current Strength and Slew Rate (cyclone V has fewer options)
- Recommended: Review Quartus compilation and fitter settings
- Compile
- Recommended: Review Quartus compilation warnings

Software Migration

While the PN4289 and PN9136 have the same PCI Device and Vendor ID's they have different PCI Sub-Device and Sub-Vendor ID's. These can be used to distinguish between the two boards.

If you are downloading the FPGA design via the PCI Bus, then we recommend using "Uncompressed Bitstreams" and downloading exactly 4,244,797 bytes. If you are using "Compressed Bitstreams", the RBF file has more bytes than are necessary to configure the FPGA. Sending extra bytes can lead to problems. We recommend that you stop 128 bytes early and then send the last bytes one by one, while checking the PLX User Register to see if the FPGA was configured after a 10us delay, to determine the exact number of bytes to send (refer to example SW).

Revisions

Rev 1 – 04/4/2019 – Initial release