Digital I/O PMC

"Tech Refresh" 32-Channel RS485/RS422 Differential PMC

The Technobox, Inc. P/N 9136 offers current 4289 users an easy way to upgrade their technology in legacy designs. All pin functionality has been retained in the 9136. A separate migration tool is provided in order to assist in renumbering the FPGA balls.

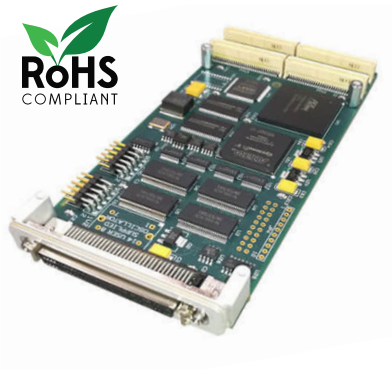
The "Tech Refresh" 32-channel reconfigurable RS422/RS485 digital I/O PMC provides a vehicle for implementing complex user-specific digital designs requiring a differential interface. This product is a third-generation design derived from the P/N 2674/3353/4289 products. All the features of the 4289 boards have been incorporated into this new product, enabling customers easy migration for existing applications.

The product uses an Intel "Cyclone V" FPGA in a 484 Fine-Line FPGA. The Intel 5CGXFC4C6F23I7N is the default FPGA on the P/N 9136 design. Older generations offered larger FPGA options to customers to increase available Logic Elements. Due to the size of the 5CGXFC-4C6F23I7N, this will no longer be necessary.

The design features a total of 32 general-purpose RS422/RS485 driven digital I/Os wired to both the front-panel and rear PN4 connector (64 signals per connector taking into account 2 signals per differential pair). For each of the 32 channels, the bidirectionality is controlled by an output from the FPGA.

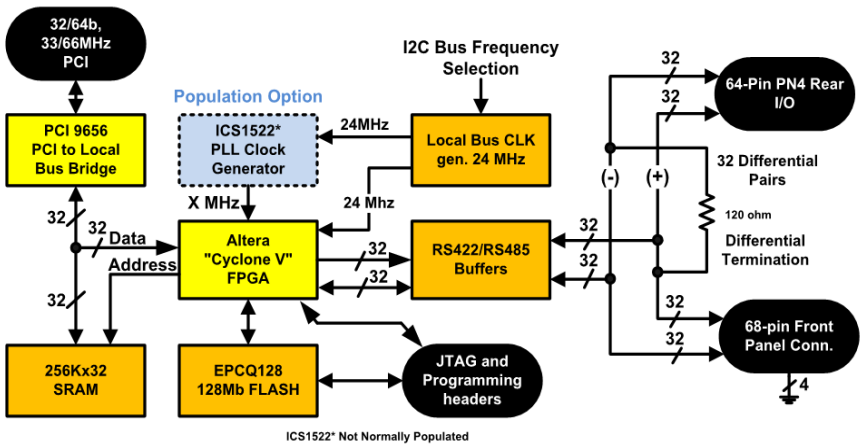
The 68-pin front-panel connector is compatible with standard fast/wide differential SCSI cables. Furthermore, optional Technobox, Inc. transition panels (e.g., P/N 3044) may be used to break out the differential signals into more convenient individual connectors, such as DB9s.

Each of the 32 differential pairs is terminated with a 120-ohm parallel resistance or an R/C termination as shown in the block diagram. Individual resistors are used with each differential pair, allowing for easy removal or value change on a per-channel basis.



9136

- **Provides 32 Channels of General-Purpose RS485/422 Digital I/O**
- **Supports 64-bit/66 MHz PCI Bus**
- **50K Logic Elements (Intel 5CGXFC4C6F23I7N "Cyclone V")**
- **Reprogrammable by Host, On-board Flash or USB Blaster Cable**
- **Local Bus SRAM (256K x 32-bit)**
- **Optional Header for Logic Analyzer Attachment**
- **Sample FPGA Design & Host "C" Code**
- **RoHS Compliant**
- **Lead-free**
- **Industrial Temp Design**



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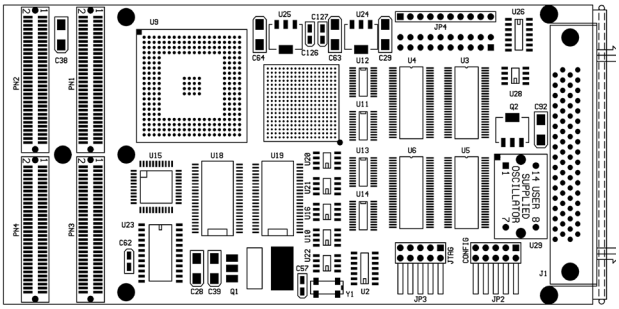
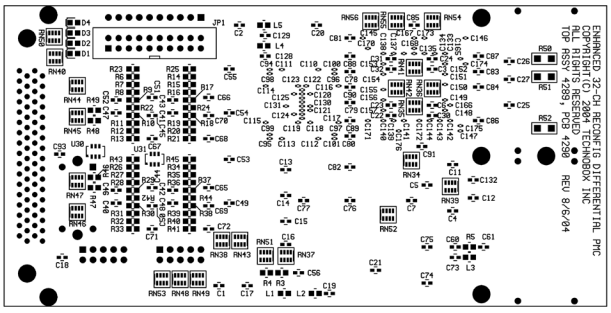


Component Placement View - Side #1



Component Placement View - Side #2

With the proper FPGA design, the 256K x 32b SRAM provided on the PMC is accessible from the Intel FPGA as well as the PCI interface.

The 32-bit data bus is shared between the Intel FPGA and the PCI interface devices. The SRAM address is driven by FPGA outputs. This technique allows a variety of memory architectures for the SRAM: single-port SRAM, dual-port SRAM, one or more FIFOs and even linked list structures for more complex applications.

For application timing, a local bus clock provides inputs to the Intel FPGA. The PLX local bus clock is set to 24MHz.

On power-up, the Intel FPGA configuration cells are automatically loaded from serial FLASH located on the PMC. The user may override the default configuration by dynamically reprogramming the FPGA from the host processor, or by in-circuit burning of the reprogrammable FLASH chip with the user's application if this is supported by the FPGA design. Also, two 10-pin headers are provided for development with USB Blaster cables. One is for the JTAG connection and the other is for programming the FLASH chip.

An example implementation of a digital I/O board with dual-port access to the SRAM and corresponding "C" source code running in the host is provided with the product. QUARTUS development software is available directly from Intel.

Specifications

Temperature (Operating): 0° to 70° C

Temperature (Storage): -40° to +85° C

Altitude: Not specified or characterized (similar equipment is at 15,000 ft.)

Humidity (Operating/Storage): 5% to 90% non-condensing

Vibration: Not specified or characterized

MTBF: 120K Hours (Gb, 20°)

Typical Power Dissipation: TBD

Power Supplies Required: +5V

PCI Environment: 5V or 3.3V; 32/64 bits, 33/66 MHz

Ordering Information

9136: (w/ 5CGXFC4C6F23I7N)*

***Standard configuration does not have the IC1522 PLL chip populated.**

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