Digital I/O PMC

96-Channel General Purpose Digital I/O

The Technobox P/N 6070 is an FPGA based PMC featuring 96 general-purpose digital I/Os distributed at the front-panel J1 connector (32 I/Os), and at the rear PN4 connector of the PMC (64 I/Os). Each group of eight I/O lines is buffered by a 74ALVC164245, and the directionality of each group is controlled by a signal from an Altera Cyclone I FPGA.

This is a reduced cost, updated and highly-compatible revision of Technobox P/N 2372 with easier to source components which should extend availability for systems now using P/N 2372. A notable difference is that P/N 6070 has a JTAG programming header for easier FPGA development.

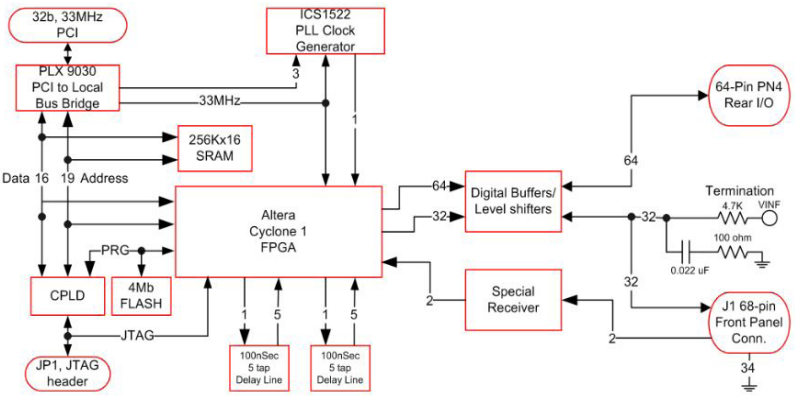
To help with moving designs from P/N 2372 to P/N 6070, Technobox offers a migration tool which translates the 10K70 FPGA pin mapping file into an EP1C4 FPGA pin mapping file.

Each of the 32 signals to the front-panel connector is terminated with an R/C parallel network for signal integrity. Termination for individual digital I/O lines may be disabled by depopulating the corresponding capacitor. The terminating voltage, VINF, can be changed from +5V to +3.3V with resistor population options, the default being +5V for compatibility with P/N 2372 designs.

The PN4 rear I/O connector is not terminated; it is anticipated that users will terminate the rear I/O signals via a suitable transition module designed for the application.

A 256K x 16 SRAM is provided on the PMC, and is accessible from the FPGA as well as the PCI interface. A dual-port RAM effect is achieved by arbitrating accesses between the FPGA and PCI bus using control logic implemented in the FPGA.

The 16-bit data bus from the PCI slave-only bridge chip, along with 19 address lines (A[18..0]),



6070

- **32-bit 33 MHz, 3.3V or 5V PCI Interface**
- **PLX PCI9030 PCI to 16-bit Local Bus Interface**
- **Supports PCI Target Only**
- **Altera Cyclone I FPGA (4K Logic Elements)**
- **12K and 20K Logic Elements FPGAs Available by Special Build**
- **Compatible Upgrade for Technobox P/N 2372**
- **Rear I/O 64 Signal**
- **Front-panel I/O 32 Signals w/ Termination**
- **Two Trigger/Clock Inputs**
- **Easily Configurable w/ Altera SOPC Builder**
- **Easily Debugged via Altera Signal Tap**
- **Configure FPGA by Serial FLASH Programming, PCI Download or JTAG Adapter**
- **RoHS-compatible**
- **Lead-free**

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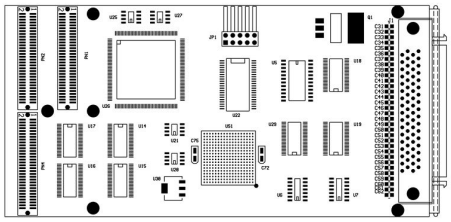
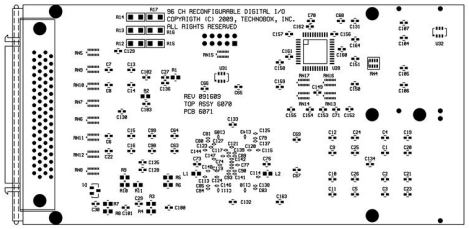


COMPONENT PLACEMENT VIEW - SIDE #1



COMPONENT PLACEMENT VIEW - SIDE #2

are con-nected to the FPGA. 32-bit PCI bus is supported, and the PCI bridge will automatically decompose 32-bit PCI accesses into multiple 16-bit equivalents as needed.

On power up, the Altera FPGA is loaded from a 4Mbit serial FLASH chip. The user may override this configuration by reprogramming the FPGA from the host processor, or the JTAG interface. The serial flash chip can also be reprogrammed with from the host interface via the user's application. The serial flash chip cannot be reprogrammed with the JTAG interface.

For application timing, the 33 MHz PCI clock and a PLL-generated clock are available for the FPGA. Any frequency with better than 0.1% accuracy can be generated by the PLL as programmed from the host processor. Also, two 100-ns delay lines with 5-taps spaced at 20 ns are available for user's time critical asynchronous needs. Finally, two special receivers are available for low-level serial clock and data recovery.

Examples of FPGA design files and "C" source code running on the host are provided in the distribution CD. This includes an example implementation of a digital I/O board with dual-port access to the SRAM. The development software is available from Altera.

SPECIFICATIONS

Temperature (Operating): -40 to +85 degrees C

Temperature (Storage): -50 to +100 degrees C

Altitude: Not Specified or Characterized. Typical similar equipment is at 15,000 ft.

Humidity (Operating/Storage): 5% to 95% non-condensing.

Vibration: Not specified or characterized

MTBF: Available on request

Typical Power Dissipation: 250 ma @ 5 Volts

Power Supplies Required: +5V

PCI Environment: 5V or 3.3V; 32 bits, 33 MHz

ORDERING INFORMATION

6070: 96-Channel General Purpose Digital I/O

6851: 12K LE Version of P/N 6070

6852: 20K LE Version of P/N 6070

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 DS6070-C10511

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