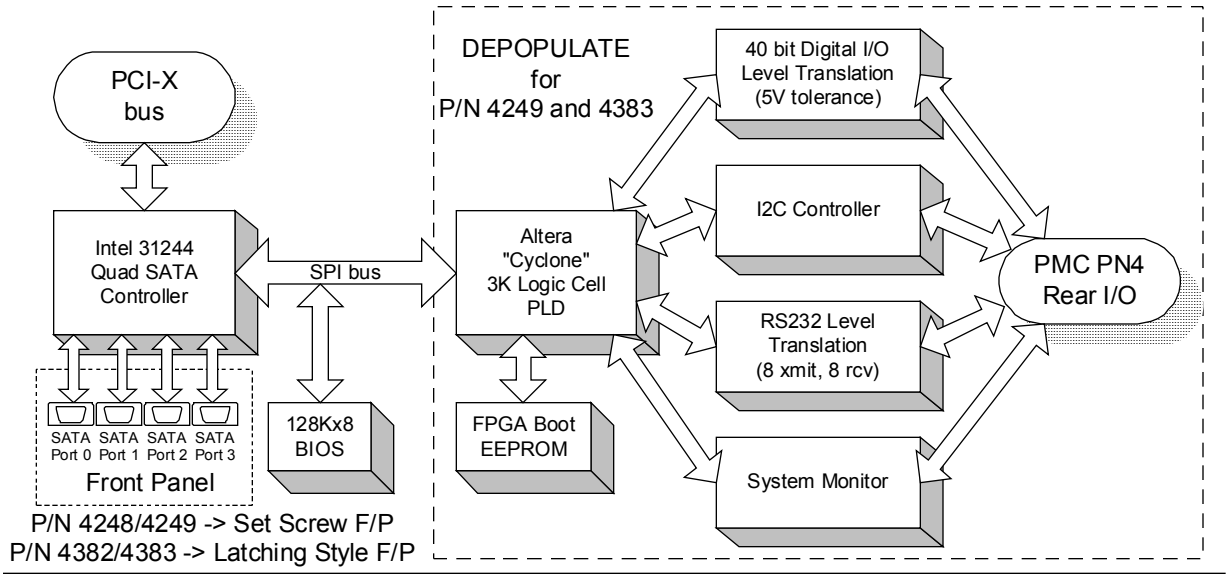
Versatile Serial ATA Controller



The "Versatile" SerialATA controller provides four 1.5Gb/s links on a PMC front panel. Additional features are provided for rear I/O as described below.

The board employs an Intel 31244 controller, which connects the PCI-X bus to four SATA links. PCI-X can operate up to 133 MHz under ideal conditions, but this board will also operate in lower speed 33-MHz and 66 MHz busses and in 32-bit and 64-bit modes. Both 5V and 3.3V PCI bus signaling is supported. For more information on the 31244 capabilities, please see www.intel.com.

The four SATA ports are accessible at the PMC front panel. Activity LEDs are provided on the front panel for each port and are located adjacent to the corresponding SATA connector. Versions are available using a proprietary "set screw" (P/Ns 4248/4249) or a more convenient "latching style" (P/Ns 4382/4383) cable connector retaining mechanism, the latter technique being endorsed by the SATA standard.

As customarily implemented with these designs, the 31244 controller uses an SPI bus to connect to a 128Kx8 EEPROM memory that holds a BIOS image. Unique to this product is the additional capability offered by an ALTERA Cyclone PLD that is hooked onto the SPI bus. Because of the serial nature of the SPI, the devices serviced by the ALTERA PLD must be used in low performance interrupt-driven applications ONLY.

The ALTERA PLD is preprogrammed with logic that supports the 31244's SPI bus, interface to an I2C controller, Four UARTs (each providing RXD, TXD, CTS, and RTS), 40 bit bits of general purpose 5V tolerant Digital I/O, and a System Monitor function. A "boot" EEPROM automatically loads the PLD on power up. Users may have access to the PLD design in order to fulfill custom logic requirements.

The peripheral devices (UARTS, I2C, System Monitor, Digital I/O) are accessed in a "shadowed" manner in the PMC's BIOS space. When the PLD detects a certain sequence of bytes and addresses to the BIOS, the PLD disconnects the BIOS chip and connects the peripheral devices, which then appear in the BIOS space.

The PLD implements four UARTS, and level translation logic on the PMC card interfaces to RS232 levels. RXD, TXD, CTS, and RTS functions are provided for each port, and are accessible at the PMC's PN4 Rear I/O connector.

40 Digital I/O lines are available at the PN4, and may be individually controlled and sensed by the host software. Each bit's directionality is programmable. The I/O uses 3.3V CMOS levels, but is 5V tolerant.

A Philips byte-wide I2C controller provides a serial interface to the PN4, consisting of serial data and serial clock. See www.philips.com for I2C information.

A "system monitor" chip on the board provides local temperature measurement, as well as remote temperature sensing via a user supplied 2N3904 diode junction. Also, the system monitor senses and reports +3.3, +5V, -12V, and +12V voltage levels provided to the board. Two 0-2.5V analog inputs are also provided on the PN4 to the system monitor chip.

For cost reduced applications only requiring the Serial ATA function, the ALTERA PLD and its associated logic can be depopulated for customer volume production run.

Contact Technobox for O/S and software support.

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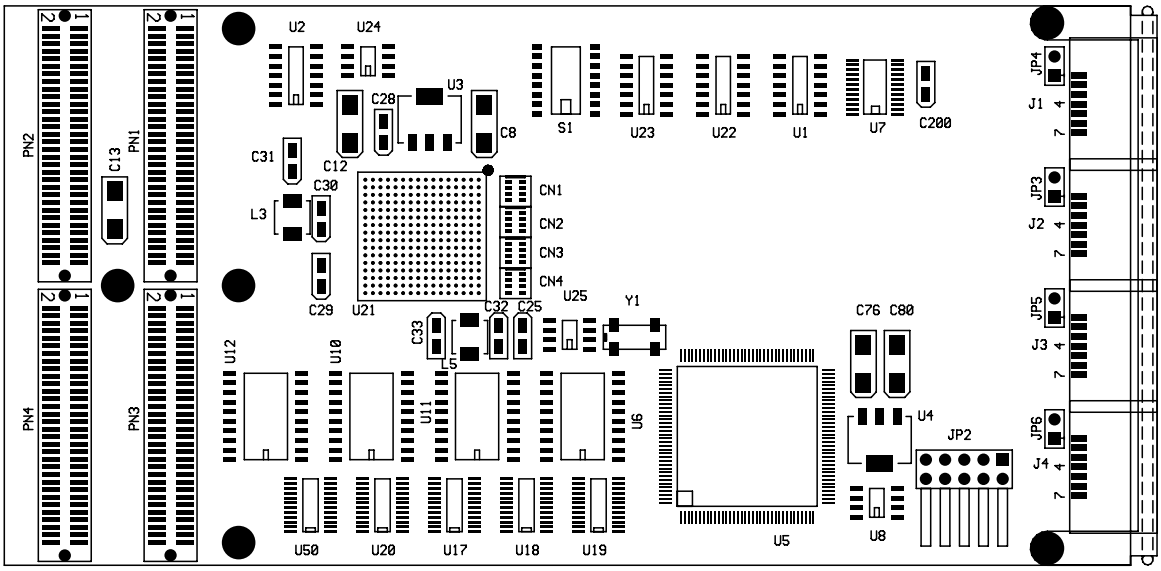

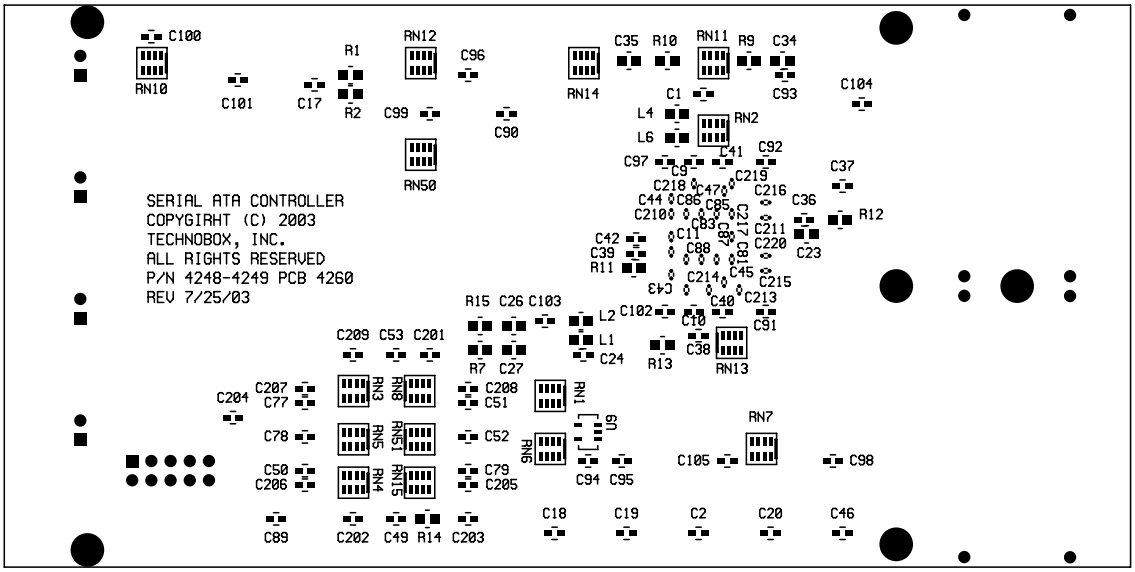

Product Summary

Technobox Part Number:	4248 (Set Screw Style F/P Fully Populated)
	4249 (Set Screw Style SATA function only. No Rear I/O)
	4382 (Latching Style conn's Fully Populated)
	4383 (Latching Style conn's SATA only. No Rear I/O)
Typical Power Dissipation:	TBD watts
Power Supplies Required:	+3.3V, +5, +12, -12
PCI Signaling Environment:	3.3V or 5V, PCI-X