Digital I/O FPGA-Based PMC

80-Channel Reconfigurable Digital I/O PMC

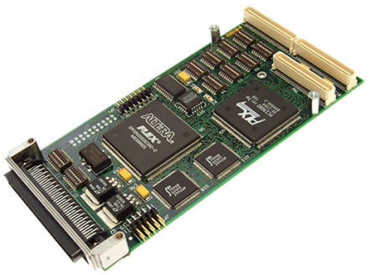
The 80-channel Reconfigurable Digital I/O PMC provides a vehicle for implementing complex user-specific digital designs requiring high-speed single-ended operation. 64 of the 80 signals are available out the PN4 connector, while all 80 signals are wired to the front-panel connector.

Each of the 80 signals are directly connected through a 56 ohm series termination resistor to pins on the ALTERA FPGA. Each pin may be an input, output, or bidirectional as determined by the ALTERA design. Also, each of the 80 signals may be hard-tied to signal GND in order to accommodate external cabling and connections that require connection to GND; this is accomplished by micro-DIP switches on the PMC module (S1-S10).

A PLX Technology 9080 part provides the interface between the PCI bus and the local bus on the PMC.The 9080 has two DMA channels and the ALTERA may request transfer by the corresponding DREQ lines to the 9080.

Programmed I/O may be used to access the ALTERA, as well as the Dual Port memory on the board. Accesses to the Dual Port RAM is via true burst 32-bit-transfers. The ALTERA internals can also be accessed with 32-bit transfers from the host, which is accomplished automatically by the 9080 using a 16-bit time-multiplexed path to the ALTERA chip. Direct addressibility of up to 2**19 bytes is provided.

The synchronous pipelined Dual Port memory is a key performance feature of this design. On one side, the dual port memory is accessed from the 9080, and burst transfers are possible using either the 9080's DMA or a bursting master on the host processor. The other side of the dual port memory is accessed by the ALTERA through separate pins for the 32-bit Data and16 address lines.



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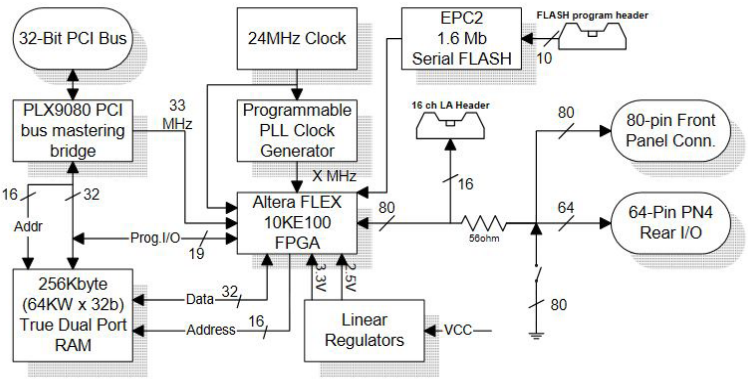

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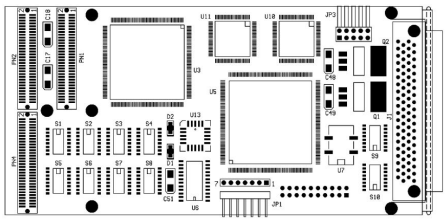
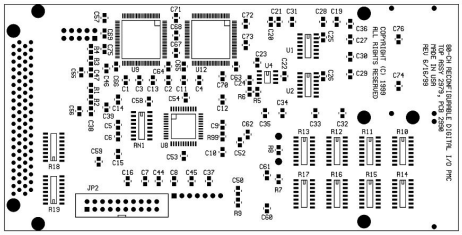


COMPONENT PLACEMENT VIEW - SIDE #1



COMPONENT PLACEMENT VIEW - SIDE #2

For application timing, the 33 Mhz from the PCI bus, 24 Mhz oscillator, and a PLL-generated clock are inputs to the Altera FPGA. Any frequency with better than 0.1% accuracy can be generated by the PLL as programmed from the host processor.

On power up, the Altera FPGA configuration cells are automatically loaded from a serial EPC2 in-circuit programmable FLASH memory located on the PMC. The user may override this default configuration by dynamically reprogramming the FPGA from the host processor, or by burning an EPC2 with the user's application.

For debug, the upper 16 bits of the 80 I/O lines are available at a 20-pin header on the reverse side of the board, which mates with an Hewlett Packard logic analyzer probe equipped with a termination adapter. Upon order, please specify if this header should be installed (default is not installed).

The product uses an Altera EPF10K100EQC240-2 Field Programmable Gate Array (FPGA) in a 240 pin Surface Mount package.

An example ALTERA implementation with corresponding "C" code is provided to serve as a foundation for the user's implementation. The Altera MAX-PLUS development software, or equivalent, is purchased directly from Altera.

SPECIFICATIONS

Typical Power Dissipation: TBD

Power Supplies Required: +5V

PCI Environment: 5V or 3.3V

ORDERING INFORMATION

2979: 80-Channel Reconfigurable Digital I/O PMC

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