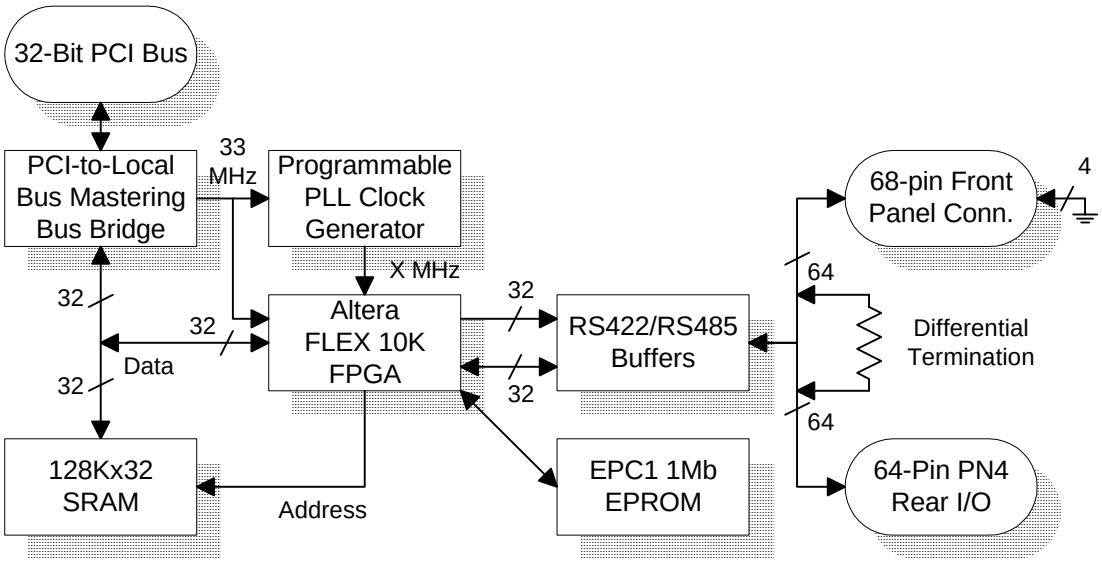
32-Channel Reconfigurable RS422/RS485 Digital I/O



The 32-channel Reconfigurable RS422/RS485 Digital I/O PMC provides a vehicle for implementing complex user-specific digital designs requiring a differential interface.

The product uses an Altera FLEX 10K Field Programmable Gate Array (FPGA) in a 240 pin Surface Mount package. The Altera FLEX 10K family in this package consists of a variety of parts from the 10K20 to the 10K70, with usable equivalent gate counts for the 10K70 from 46K to 118K gates for representative designs.

The EPF10K70RC240-4 is used for the default configuration, which provides the highest gate count at reasonable speeds. For volume production runs, other lower density and/or higher speed parts may be substituted.

The design features a total of 32 general-purpose RS422/RS485 driven digital I/Os wired to both the front panel and rear PN4 connector (64 signals per connector taking into account 2 signals per differential pair). The bidirectionality for each of the 32 channels is controlled by an output from the FLEX10K part.

The 68-pin front panel connector is compatible with standard fast/wide differential SCSI cables. Furthermore, a optional Technobox transition panel (e.g., P/N 1867) may be used to break out the differential signals into more convenient individual connectors, such as DB9s.

I/O out the PMC front panel is terminated with a parallel resistance as shown. Termination for individual differential I/O lines may be disabled by de-populating the corresponding resistor.

With the proper ALTERA design the 128K x 32b SRAM provided on the PMC is accessible from the Altera part as well as the PCI interface. The 32-bit data bus is shared between the ALTERA and the PCI interface devices. The SRAM address is driven by ALTERA outputs. This technique allows a variety of memory architectures for the SRAM: single-port SRAM, dual-port SRAM, one or more FIFOs, and even linked list structures for more complex applications.

For application timing, the 33 Mhz from the PCI bus and a PLL-generated clock are inputs to the Altera FPGA. Any frequency with better than 0.1% accuracy can be generated by the PLL as programmed from the host processor.

On power up, the Altera FPGA configuration cells are automatically loaded from a serial EPROM located on the PMC. The user may override this default configuration by dynamically reprogramming the FPGA from the host processor, or by burning an EPC1 with the user's application (EPC1 chips and programmer are not supplied).

An example implementation of a digital I/O board with dual-port access to the SRAM, implemented in Altera HDL ("AHDL"), and corresponding "C" source code running in the host is provided with the product. The Altera MAX-PLUS development software, or equivalent, is purchased directly from Altera.

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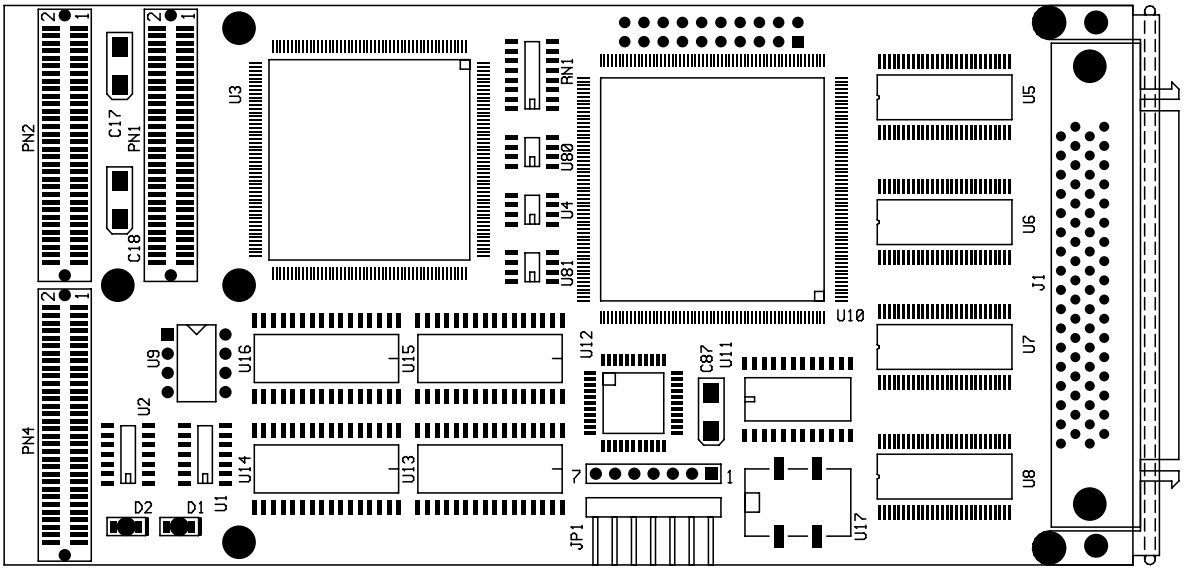

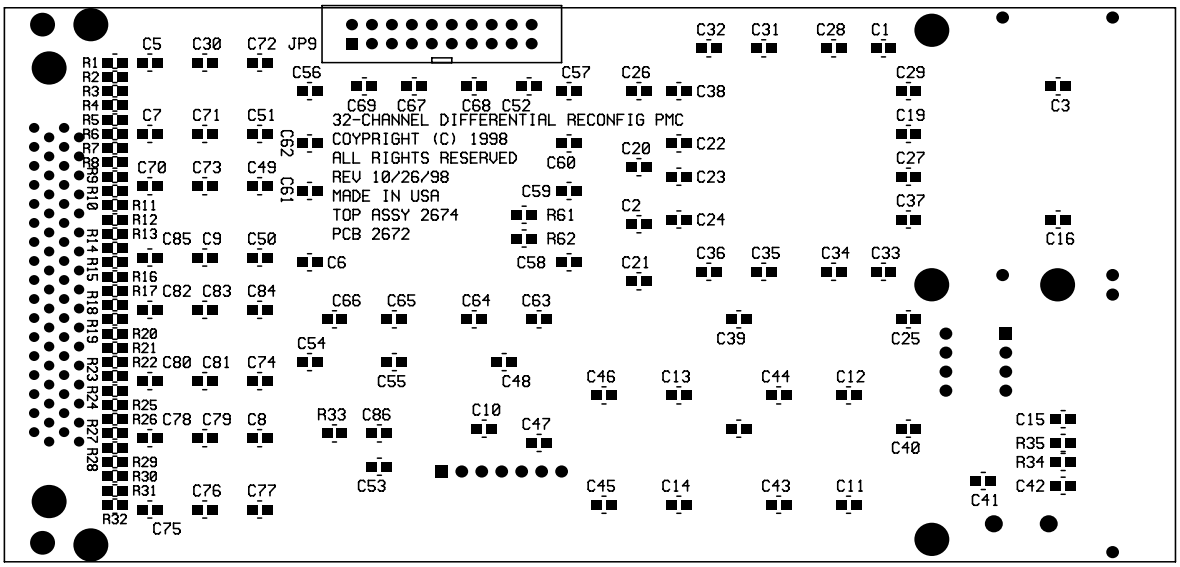

Product Summary

Technobox Part Number:	2674
Typical Power Dissipation:	TBD
Power Supplies Required:	+5V
PCI Signaling Environment:	5V or 3.3V